

Applicant(s):

George Matamis et al.

Title:

Bitline Direction Shielding to Avoid Cross Coupling Between Adjacent

Cells for NAND Flash Memory

Application No.:

10/680,665

Filing Date:

October 6, 2003

Examiner:

Unassigned

Group Art Unit:

Unassigned

Docket No.:

SNDK.294US0

Conf. No.:

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Certificate of Mailing Under 37 CFR 1.8

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Kathy Joinston

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Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application.

Citation of these documents shall not be construed as:

- 1. an admission that the documents are necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made, a representation that a search has been made, (other than as indicated by any cited document); or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in $\S 1.56(b)$.

1/14/03

Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office Application No. Atty. Docket No. INFORMATION DISCLOSURE STATEMENT BY SNDK.294US0 10/680,665 APPLICANT Applicant(s) se several sheets if necessary) George Matamis et al. NOV 2 4 200 Filing Date Group October 6, 2003 Unknown **U.S. Patent Documents** Document Filing Date Initial Number Date Subclass Name Class If Appropriate 8/1991 001 5,043,940 Harari 002 5,070,032 12/1991 Yuan 003 5,095,344 3/1992 Harari 004 5,168,465 12/1992 Harari 12/1992 005 5,172,338 Mehrotra 006 5,198,380 3/1993 Harari 007 5,268,318 12/1993 Harari 800 5,268,319 12/1993 Harari 009 5,313,421 Guterman 5/1994 010 5,343,063 8/1994 Yuan 011 5,380,672 1/1995 Yuan 012 5,512,505 4/1996 Yuan Yuan 013 7/1996 5,534,456 014 5,554,553 9/1996 Yuan 015 5,579,259 11/1996 Samachisa 016 5,595,924 1/1997 Yuan 017 5,654,217 8/1997 Yuan 018 5,661,053 8/1997 Yuan 019 5,677,872 Samachisa 10/1997 020 5,712,179 1/1998 Yuan 021 5,747,359 5/1998 Yuan OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Y. Takeuchi et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit 022 Flash Memories," 1998 Symposium on VLSI Technology - Digest of Technical Papers, June 9-11, 1998, Seiichi Aritome, "Advanced Flash Memory Technology and Trends for File Storage Application," 2000 023 International Electron Devices Meeting, December 10-13, 2000, pp. 33.1.1-33.1.4. Examiner Date Considered *EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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				Filing Date			Group
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